Electronic Version
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Claims

[c1] What is claimed is:

1.A method of measuring a gate channel length of a metal-oxide semiconductor transistor (MOS transistor) on a silicon substrate comprising:

forming a first MOS transistor, the first MOS transistor comprising a first gate with a known channel length and a known channel width, within a first region on a surface of the silicon substrate;

forming a second MOS transistor, the second MOS transistor comprising a second gate with an unknown channel length and a known channel width, within a second region on the surface of the silicon substrate;

applying a predetermined voltage on both the first gate and the second gate;

measuring a first inverse gate leakage current of the first MOS transistor and a second inverse gate leakage current of the second MOS transistor; and

using the first inverse gate leakage current, the second inverse gate leakage current, the channel widths of the first and the second gates, the channel length of the first gate and an equation to obtain the channel length of the second gate.

[c2] 2.The method of claim 1 wherein the first and the second gate respectively comprise a first gate oxide layer and a second gate oxide layer, the first gate oxide layer having a thickness equal to a thickness of the second gate oxide layer.

[c3] 3.The method of claim 2 wherein the thicknesses of the first and the second gate oxide layers are both less than 20 angstroms.

[c4] 4.The method of claim 1 wherein the first and second MOS transistors are both P-type MOS transistors.

[c5] 5.The method of claim 4 wherein the predetermined voltage is less than 2 volts.

[c6] 6.The method of claim 1 wherein the first and second MOS transistors are both N-type MOS transistors.

[c7] 7.The method of claim 6 wherein the predetermined voltage is greater than 2 volts.

[c8] 8.The method of claim 1 wherein the equation is expressed as follows:

$Ig_1 \div (W_1 \times L_1) = Ig_2 \div (W_2 \times L_2)$

wherein Ig_1 and Ig_2 respectively represent the first and second inverse gate leakage currents, W_1 and W_2 respectively represent the channel widths of the first and sec-

ond gets, and L_1 and L_2 respectively represent the channel lengths of the first and the second gates.

[c9] 9.The method of claim 1 wherein the first region is within a scribe line area on the surface of the silicon substrate, and the second region is within an active area on the surface of the silicon substrate.

[c10] 10.The method of claim 1 wherein the first region is within a test key area on the surface of the silicon substrate.

[c11] 11.A method of measuring a gate channel length of a MOS transistor on a silicon substrate comprising:
forming a first MOS transistor, the first MOS transistor comprising a first gate with a known channel length and a known channel width, and a second MOS transistor, the second MOS transistor comprising a second gate with an unknown channel length and a known channel width, respectively within a first region and a second region on a surface of the silicon substrate;
applying a predetermined voltage on both the first gate and the second gate; and
measuring a first inverse gate leakage current of the first MOS transistor and a second inverse gate leakage current of the second MOS transistor;
wherein the channel length of the second gate is equal

to $(Ig_2 \times W_1 \times L_1) \div (Ig_1 \times W_2)$, wherein Ig_1 and Ig_2 respectively represent the first and second inverse gate leakage currents, W_1 and W_2 respectively represent the channel widths of the first and second gets, and L_1 represents the channel length of the first gate.

[c12] 12.The method of claim 11 wherein the first and the second gate respectively comprise a first gate oxide layer and a second gate oxide layer, the first gate oxide layer having a thickness equal to a thickness of the second gate oxide layer.

[c13] 13.The method of claim 12 wherein the thicknesses of the first and the second gate oxide layers are both less than 20 angstroms.

[c14] 14.The method of claim 11 wherein the first and second gates are gates of two different P-type MOS transistors.

[c15] 15.The method of claim 14 wherein the predetermined voltage is less than 2 volts.

[c16] 16.The method of claim 11 wherein the first and second gates are gates of two different N-type MOS transistors.

[c17] 17.The method of claim 16 wherein the predetermined voltage is greater than 2 volts.

[c18] 18.The method of claim 11 wherein the first region is

within a scribe line area on the surface of the silicon substrate, and the second region is within an active area on the surface of the silicon substrate.

[c19] 19.The method of claim 11 wherein the first region is within a test key area on the surface of the silicon substrate.